19. (New) A semiconductor device comprising:

a wiring substrate having a main surface, a rear surface opposed to the main surface, a first row of electrode pads on the main surface, a plurality of lands formed on the rear surface and a plurality of wirings electrically connected to the electrode pads with the lands, respectively;

a first semiconductor chip having a main surface, a rear surface opposed to the main surface, a plurality of electrode pads formed on the main surface, wherein the first semiconductor chip is mounted on the main surface of the wiring substrate with the rear surface of the first semiconductor chip facing to the main surface of the wiring substrate;

a second semiconductor chip having a main surface, a rear surface opposed to the main surface, a plurality of electrode pads formed on the main surface, wherein the second semiconductor chip is mounted on the main surface of the wiring substrate at the opposed side of the first semiconductor chip from the first row of electrode pads with the rear surface of the first semiconductor chip facing to the main surface of the wiring substrate;

a plurality of wires electrically connecting the electrode pads of the first semiconductor chip and the first row of electrode pads, respectively; and

a sealing material sealing the first and second semiconductor chips and the plurality of wires;

wherein an angle between the main surface of the wiring substrate and the wires at a portion of connecting the first row of electrode pads is larger than an angle between the main surface of the first semiconductor chip and the wires at a portion of connecting the electrode pads of the first semiconductor chip.

20. (New) A semiconductor device according to claim 19, further comprising:

a second row of electrode pads formed on the main surface of the wiring substrate, between the first semiconductor chip and the second semiconductor chip in plan; and

a plurality of wires electrically connecting the electrode pads of the second semiconductor chip and the second row of electrode pads, respectively;

wherein an angle between the main surface of the wiring substrate and the wires at a portion of connecting the second row of electrode pads is larger than an angle between the main surface of the second semiconductor chip and the wires at a portion of connecting the electrode pads of the second semiconductor chip.